

REMARKS

Claims 1-15, and 17-22 are presented for further examination. Claim 16 has been canceled. Claims 1, 7, and 12 have been amended. Claims 21 and 22 are new.

In the Office Action dated September 25, 2003, the Examiner rejected claims 1-4, 7, 9-12, and 14-17 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,034,958 (“Wicklund”). Claims 5, 6, 8, 13, and 18 were objected to but found to be allowable as rewritten into independent form. Claims 19 and 20 were found to be allowable.

Applicant respectfully disagrees with the basis for the rejection and requests reconsideration and further examination of the claims.

Wicklund, U.S. Patent No. 6,034,958 is directed to a VP/VC lookup function that utilizes task coding and binary table search techniques. More particularly, Wicklund provides a circuit (Hash coder 204) that generates a pack address (Hash code 14) by dividing a current Phy/Vpi/Vci address by a polynomial (see Wicklund, column 5, lines 42-50). Wicklund does not teach or suggest suppressing in the address bits having “predetermined positions.” In other words, the polynomial has variables ( $X^{14}+X^{13}+X^{11}+X^9+1$  (see Wicklund, column 5, line 51)), where the variables do not correlate in any way to predetermined bits. Thus, a packed address generated by a polynomial division of an address cannot be compared to a packed address generated by a simple suppression of predetermined bits in an address. Moreover, Wicklund describes Hash coding as a fundamental feature, and in fact it is claimed in every claim of Wicklund, thus teaching away from replacing the hash coder by a packing circuit as recited in claim 1.

More particularly, claim 1 recites a device for associating indexes to addresses chosen from a greater number of values than a number of available indexes, including a memory containing indexes and respective check words corresponding to bits and a packing circuit receiving a current address and suppressing in this address bits *having the predetermined positions*. Claim 1 further recites a comparator configured to indicate that the current address

corresponds to the selected memory location when the bits of the check word are equal to the corresponding bits of the corresponding address. As discussed above, nowhere does Wicklund teach or suggest having check words corresponding to bits having predetermined positions in the addresses associate with the indexes and packing the current address and suppressing in the address bits having the predetermined positions. In view of the foregoing, applicant submits that claim 1 as well as dependent claims 2-6 are allowable over Wicklund.

Independent claims 7 and 12 each recite, *inter alia*, a packing circuit that reduces the number of address bits to a packed address by suppressing from the address check word bits having predetermined positions in the address bits. Applicant submits that independent claims 7 and 12, as well as all claims depending therefrom, are allowable over Wicklund for the reasons discussed above with respect to claim 1.

New claims 21 and 22 correspond to allowable dependent claims 8 and 13 rewritten into independent form to include the limitations of the base claim and any intervening claims. Applicant submits that claims 21 and 22 are allowable in view of the allowance of dependent claims 8 and 13.

Applicant respectfully submits that all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,  
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